REMARKS

I. Summary of Office Action

Claims 1-37 are pending in this application.

Claims 1-4, 8, 16-20, 25-34, and 36-37 are rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Chaudhary U.S. Patent No. 5,889,411 (hereinafter "Chaudhary").

Claims 1-2 and 9 are rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Rupp U.S. Patent No. 6,633,181 (hereinafter "Rupp").

Claims 21-24 are rejected under 35 U.S.C. § 103(a) as allegedly being obvious from Chaudhary in view of Park et al. U.S. Patent No. 6,359,468 (hereinafter "Park").

Claims 5-7, 10-15, and 35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

II. Summary of Applicant's Reply

Applicant has amended claims 1, 3, 4, 25, and 32 to more clearly define the claimed invention. No new matter has been introduced and the amendments are fully supported by the specification.

Applicant notes with appreciation the indication of allowable subject matter in claims 5-7, 10-15, and 35. Applicant has rewritten claims 5, 10, 13, and 35 in independent form to include all of the limitations of the claim's respective base claims and intervening claims. Applicant submits that claims 6-7, 11-12, and 14-15, which depend from one of rewritten claims 5, 10, and 13, are allowable at least because they depend from allowable claims.

The Examiner's rejections of claims 1-4, 8-9, 16-34, and 36-37 are respectfully traversed.

III. Applicant's Reply to the § 102 Rejections

Claims 1-4, 8, 16-20, 25-34, and 36-37 are rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Chaudhary. Claims 1-2 and 9 are rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Rupp. These rejections are respectfully traversed.

A. The Rejections of Claims 1-4, 8-9, 16-20, and 25-31

Amended independent claims 1 and 25 are directed towards circuitry and methods related to logic modules including at least three serial stages, wherein each of the stages receives at an input at least one input signal of the logic module. XOR circuitry is interposed between two of the stages or between a third stage and an output. As amended, the logic modules include multiplexer circuitry for producing a carry out signal by selecting one of the carry in signal and an output signal of one of the stages of the combinational logic circuitry as the carry out signal.

Chaudhary describes a configurable logic element having internal logic for generating wide XOR functions. The Office Action alleges that Chaudhary's function generators H and J are first and second stages of circuitry, and that multiplexers 82H and 82J are a third stage of circuitry in accordance with the claimed invention. However, function generators H and J and multiplexers 82H and 82J are not coupled in series, and thus cannot be first, second and third serial stages as claimed.

Furthermore, multiplexers 82H and 82J do not receive at an input at least one input signal of the logic module, as required by amended claims 1 and 25. Instead, the

multiplexers may receive at their inputs fixed logic values (logic 1, logic 0), logic signals produced by logic gates 61J and 61H, or signals produced by module circuitry elements. Because multiplexers 82H and 82J do not receive at their input at least one input signal of the logic module, the multiplexers cannot be first, second or third serial stages of circuitry receiving at least one input signal of the logic module in accordance with applicant's invention.

In addition, Chaudhary does not show multiplexer circuitry for producing a carry out signal by selecting one of the carry in signal and an output of one of the stages of the combinational logic circuitry, as required by claims 1 and 25. The Office Action alleges that multiplexers CJ and CH may produce the claimed carry out signal. However, multiplexers CJ and CH cannot select an output of one of the claimed stages of circuitry as a carry out signal at least because neither of multiplexers CJ and CH have a selection input coupled to a first, second or third serial stage of circuitry in accordance with the invention.

For at least these reasons, applicant submits that amended claims 1 and 25, and dependent claims 2-4, 8-9, 16-24, and 26-31, which depend from one of claims 1 and 25, are novel in view of Chaudhary. Applicant respectfully requests that the rejection of claims 1-4, 8-9, and 16-31 in view of Chaudhary be withdrawn.

The Office Action further alleges that claims 1-2 and 9 are anticipated by Rupp. Rupp describes a programmable logic array including various types of functional blocks. The Office Action contends that Rupp's selection blocks 702, 704 and 710 are first, second and third stages in accordance with applicant's claim 1. Applicant submits that Rupp's selection blocks 702 and 704 are not coupled in series, and

therefore that blocks 702, 704 and 710 cannot be first, second and third serial stages as claimed. In addition, block 710 does not receive at an input at least one input signal of the module circuitry in accordance with applicant's invention. Block 710 thus cannot be one of the first, second, or third serial stages of circuitry receiving an input signal of the logic module. Finally, Rupp does not disclose multiplexer circuitry for producing a carry-out signal as required by claim 1.

For at least the above reasons, applicant submits that claim 1, and claims 2 and 9 which depend from claim 1, are novel in view of Rupp. Applicant respectfully requests that the rejection of claims 1-2 and 9 in view of Rupp be withdrawn.

B. The Rejection of Claims 32-34

Amended independent claim 32 is directed towards logic module circuitry comprising look-up table circuitry having first, second, third and fourth serial stages, each of the stages receiving at an input at least one input signal of the logic module circuitry. XOR circuitry produces further signal information from a carry in signal and a combinational logic signal. As amended, the logic module circuitry includes multiplexer circuitry for producing a carry out signal by selecting one of the carry in signal and an output signal of one of the stages of the look-up table circuitry as the carry out signal.

The Office Action alleges that Chaudhary's function generators H and J, multiplexers DJ and DH, and registers RV and RZ are first, second, third and fourth stages in accordance with the claimed invention. However, Chaudhary's elements H, J, DJ and DH, and RV and RZ are not coupled in

series, and thus cannot be first, second, third and fourth serial stages as required by claim 32.

In addition, Chaudhary does not show multiplexer circuitry for producing a carry out signal by selecting one of the carry in signal and an output of one of the stages of the look-up table circuitry, as required by claim 32.

For at least the above reason, applicant submits that amended claim 32, and claims 33-34 which depend from claim 32, are novel in view of Chaudhary. Applicant respectfully requests that the rejection of claims 32-34 in view of Chaudhary be withdrawn.

IV. Applicant's Reply to the § 103 Rejection

Claims 21-24 are rejected under 35 U.S.C. § 103(a) as allegedly being obvious from Chaudhary in view of Park. Applicant has shown independent claim 1 to be allowable. Claims 21-24, which depend from claim 1, are allowable at least because they depend from an allowable claim. Applicant respectfully requests that the rejection of claims 21-24 be withdrawn.

V. Conclusion

In view of the foregoing, claims 1-37 are in condition for allowance. Reconsideration and allowance of this application are accordingly respectfully requested.

Respectfully submitted,

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